Remarks

Applicants respectfully request reconsideration of this application as amended. No claims have been amended. No claims have been canceled. Therefore, claims 1-28 and 38-49 are now presented for examination.

In the Final Office Action, claims 1-28 and 38-49 stand rejected under 35 U.S.C. 102(b) as being clearly anticipated by Direct Rambus Technology Disclosure ("Rambus Disclosure"). Applicants submit that the present claims are patentable over the Rambus Disclosure.

The Rambus Disclosure discloses a memory controller coupled to Rambus DRAMs via a Rambus Channel. The memory controller contains intelligence and a Rambus Interface that converts from low-swing voltage levels used by the Rambus Channel to ordinary CMOS logic levels. See Rambus Disclosure at page 7, column 2. In addition, the Rambus memory controller supports all control functions including protocol, refresh, memory and interleaving support (page 14, col. 2). Nevertheless, the Rambus Disclosure does not disclose or suggest a memory controller comprising a refresh timing circuit for generating clock pulses used to trigger memory refreshes.

Claim 1 recites:

> A computer system comprising:
> a memory; and
> memory controller, wherein the memory controller includes a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

The Rambus Disclosure simply describes a memory controller that supports refreshes. However, the disclosure of a memory controller with refresh control is not analogous, nor implicit, of a memory controller having a refresh timing circuit for generating clock pulses used to trigger memory refreshes. The Examiner asserts that:

> [T]he Rambus memory controller is a controller for dynamic RAM (DRAM) which inherently requires refreshing in order to maintain coherency of the stored

> data. On page 14 of the reference it is states that the RMC supports all control functions including protocol, refresh memory and interleaving support. In order to support refresh functions clock pulses must be used to trigger memory refreshes necessary for DRAM. It is admitted that there is not a great deal of details given in relationship to refresh functions . . .

(See Final Office Action at page 2, paragraph 4).

Applicants submit, however, that although the RMC may control refreshing using clock function triggers, no timing circuitry is disclosed that generates the clock pulses that trigger the refresh. Moreover, applicants submit that for anticipation under 35 U.S.C. 102(b), a reference must teach every aspect of the claimed invention either explicitly or inherently. The Examiner admits that the Rambus Disclosure does not disclose refresh timing circuitry, and relies upon the RMC inherently disclosing such circuitry.

However, it is not inherent that a memory controller includes refresh timing circuitry. In fact prior art memory controllers, such as the RMC disclosed in the Rambus Disclosure, receive clock pulses from an external clock source in order to trigger a memory refresh. See page 3, lines 6-11 of applicants Background section. Receiving clock pulses from an external clock source requires an additional pin to be used that may lead to an increase in circuit complexity (page 3, lines 12-19). Consequently, claim 1 is patentable over the Rambus Disclosure.

Claims 2-15 depend from claim 1 and include additional limitations. Therefore, claims 2-15 are also patentable over the Rambus Disclosure.

Claim 16 recites:

> A memory controller comprising:
> a refresh timing circuit for generating clock pulses used to trigger memory refresh events.

Thus, for the reasons stated above with respect to claim 1, claim 16 is also patentable over the Rambus Disclosure. Because claims 17-28 depend from claim 16 and

include additional limitations, claims 17-28 are also patentable over the Rambus Disclosure.

Claim 38 recites:

> A refresh timing circuit comprising:
> an internal clock generator;
> a first counter coupled to the clock generator;
> a storage register coupled to the clock generator and the counter; and
> a comparator coupled to the clock generator, the counter and the storage register.

Thus, for the reasons stated above with respect to claim 1, claim 38 is also patentable over the Rambus Disclosure. Since claims 39-49 depend from claim 28 and include additional limitations, claims 39-49 are also patentable in view of the Rambus Disclosure.

Applicants respectfully submit that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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